Amendments to the specifications

Please replace the paragraph beginning on page 2 line 13 with the following paragraph:

Fig. 3 shows a conventional CMOS image sensor chip. The image pixel area, 20, can occupy about 90% of the chip area. This area, usually arranged in the form of a grid matrix array as shown, contains photodiode regions, 48, which take up most of the area and the remaining sensor circuitry, which are placed in the areas 50, peripheral to the photodiodes. Logic circuits are contained in the chip peripheral area, 22, which also contains metal regions, 24 used for interconnection. Logic circuits require up to five levels of metal. The layered structure of an image pixel region of a CIS is shown in Fig.4. A photodiode, [[28]] 70, is situated under a shallow trench isolation region, 30, and other components are included in region 32. All these regions are contained in or on a semiconductor substrate, 54. Only the two metal levels, 26 and 28 are required for interconnection in the image pixel region. These interconnection metal levels do not completely shield the underlying sensor devices from incoming light, which gives rise to extraneous currents and noise that affects the performance of the devices. Furthermore, the two interconnection metal levels are insufficient to adequately collimate incoming light and there is cross talk to nearby sensors, as indicated in Fig.4, 46.

Please replace the paragraph beginning on page 6 line 9 with the following paragraph:

The structure of a preferred embodiment of the new grid metal design for CMOS image sensor chips is shown in Fig. 5, which depicts the layout and in Fig. 6, in

which is shown the layered structure of the pixel area. In the new grid metal design the photodiode peripheral areas, which in the conventional design, 50, are sparsely covered by two levels, 26 and 28, of interconnection metal, are completely covered by additional full levels of metal, 52. As in conventional CMOS image sensor chips the image pixel area, 20 can occupy about 90% of the chip area. This area, usually arranged in the form of a grid matrix array as shown, contains photodiode regions, 48, which take up most of the area and the remaining sensor circuitry, which are placed in the areas 50, peripheral to the photodiodes. Logic circuits are contained in the chip peripheral area, 22, which also contains metal regions, 24. Dummy metal patterns are added to completely cover the region peripheral to the photodiodes. These dummy metal patterns are therefore disposed over the functional metal levels of the image sensors and over the image sensor circuit elements other than the photodiode, these features being placed in the regions peripheral to the photodiodes. Generally, only two levels of metal are used, for interconnection, in the image pixel regions, while five levels of metal, shown in Fig.6 as 80, 82, 84, 86 and 88, are often required for the logic circuits, 90, placed in the chip peripheral area. Three levels of metal are thus available, essentially for free, for the dummy metal patterns in the image pixel region, and these are the three metal levels, 56,58 and 60 are the dummy patterns of preferred embodiments of the invention. The area of the dummy metal patterns is much larger than that of the metal levels of the peripheral logic circuits. The exposed surface area of the dummy metal levels does not change appreciably during metal etch and consequently there is only a small fractional change during metal etch in the exposed metal surface area of the chip. The loading affects during

metal etching are therefor alleviated. With complete metal coverage of the photodiode peripheral regions, the image sensor circuits other than the photodiodes, which are contained in these regions, are well shielded from the incoming light. In a conventional CMOS image sensor the pixel interconnection metal levels do not completely shield the underlying sensor devices from incoming light, which can result in extraneous currents and noise that affects the performance of the devices. With the new grid metal design of the invention, which includes complete metal coverage of the photodiode peripheral regions that shields the sensor devices from incoming light, these extraneous current and noise are not generated. Furthermore, the two interconnection metal levels are insufficient to adequately collimate incoming light and there is cross talk to nearby sensors, as indicated in Fig.4, 46. In preferred embodiments of the invention three dummy metal patterns are added to the two functional metal levels in the image pixel regions. These provide five levels of metal that adequately collimate incoming light and prevent cross talk to nearby sensors, as indicated in Fig.6.